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LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

8L PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SGND1
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : SGND2
LAYER 8 : BOT

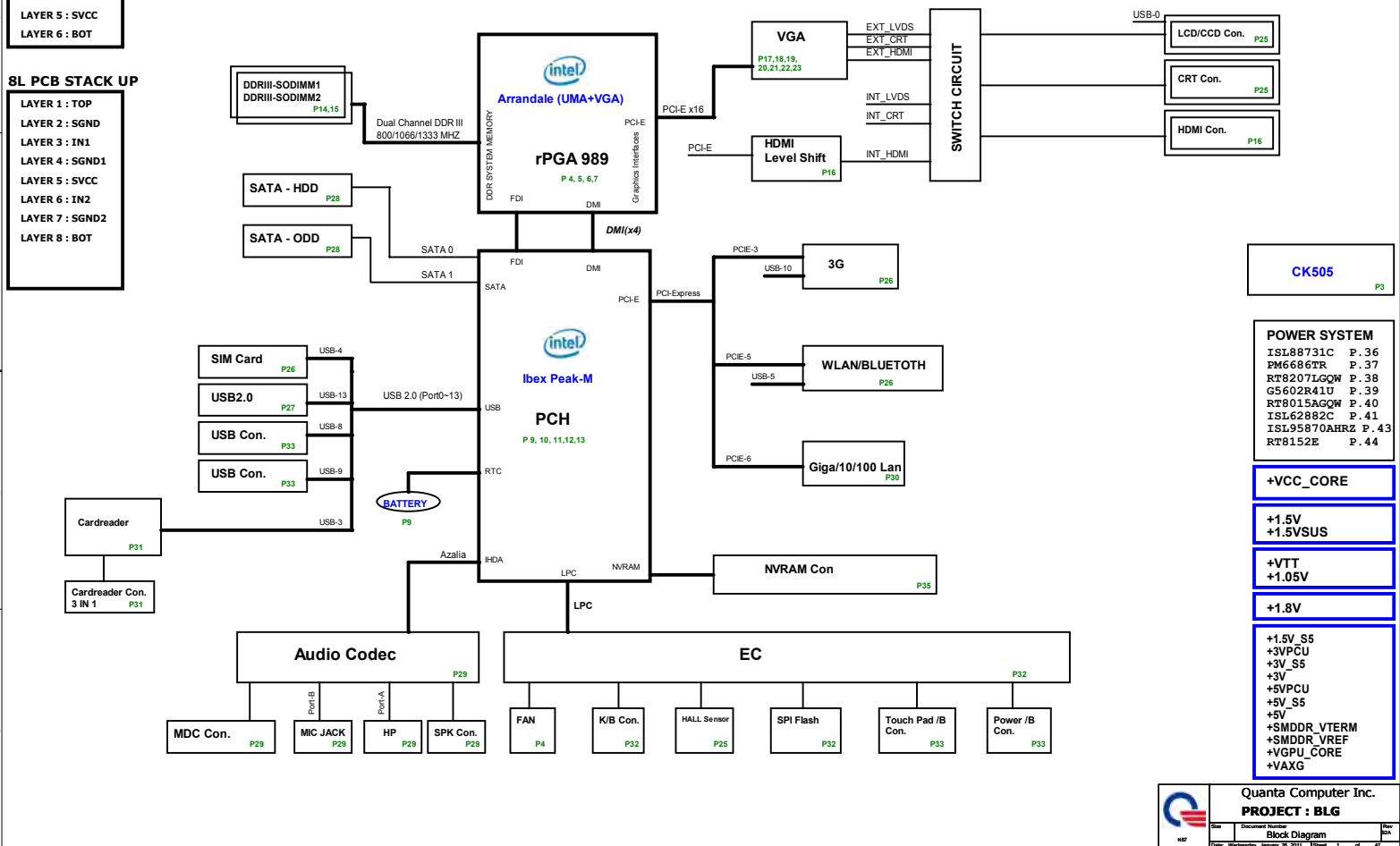



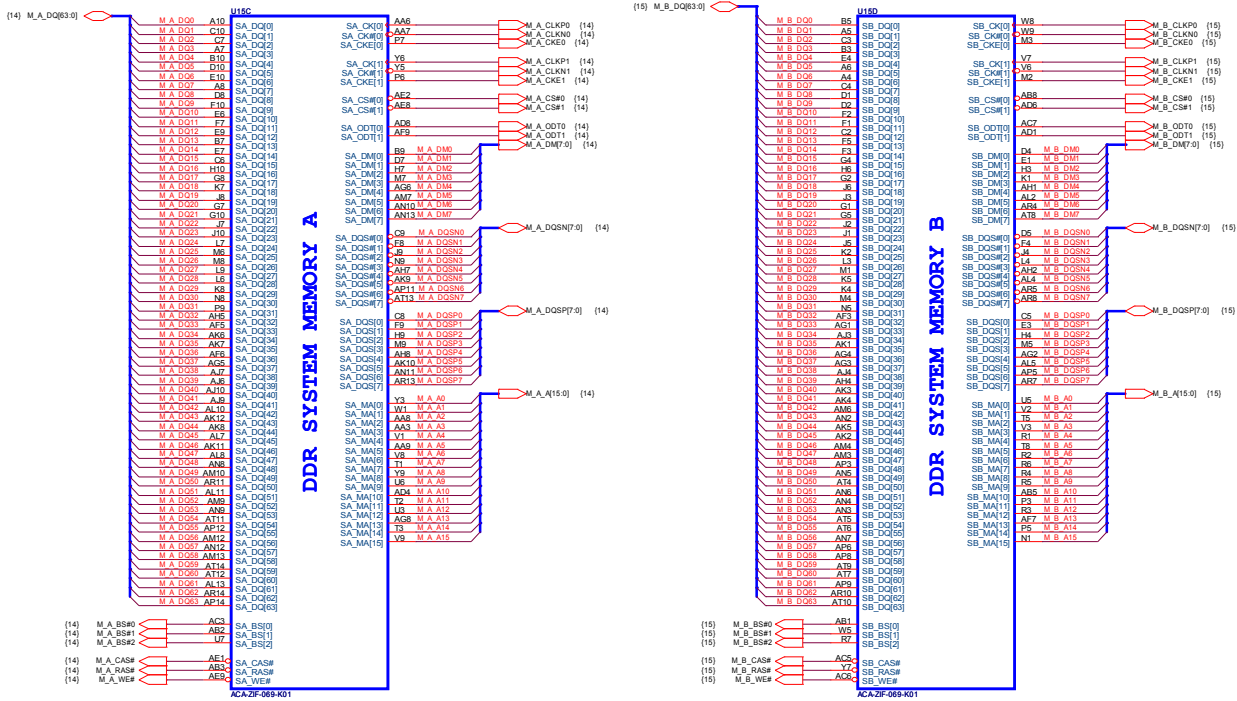


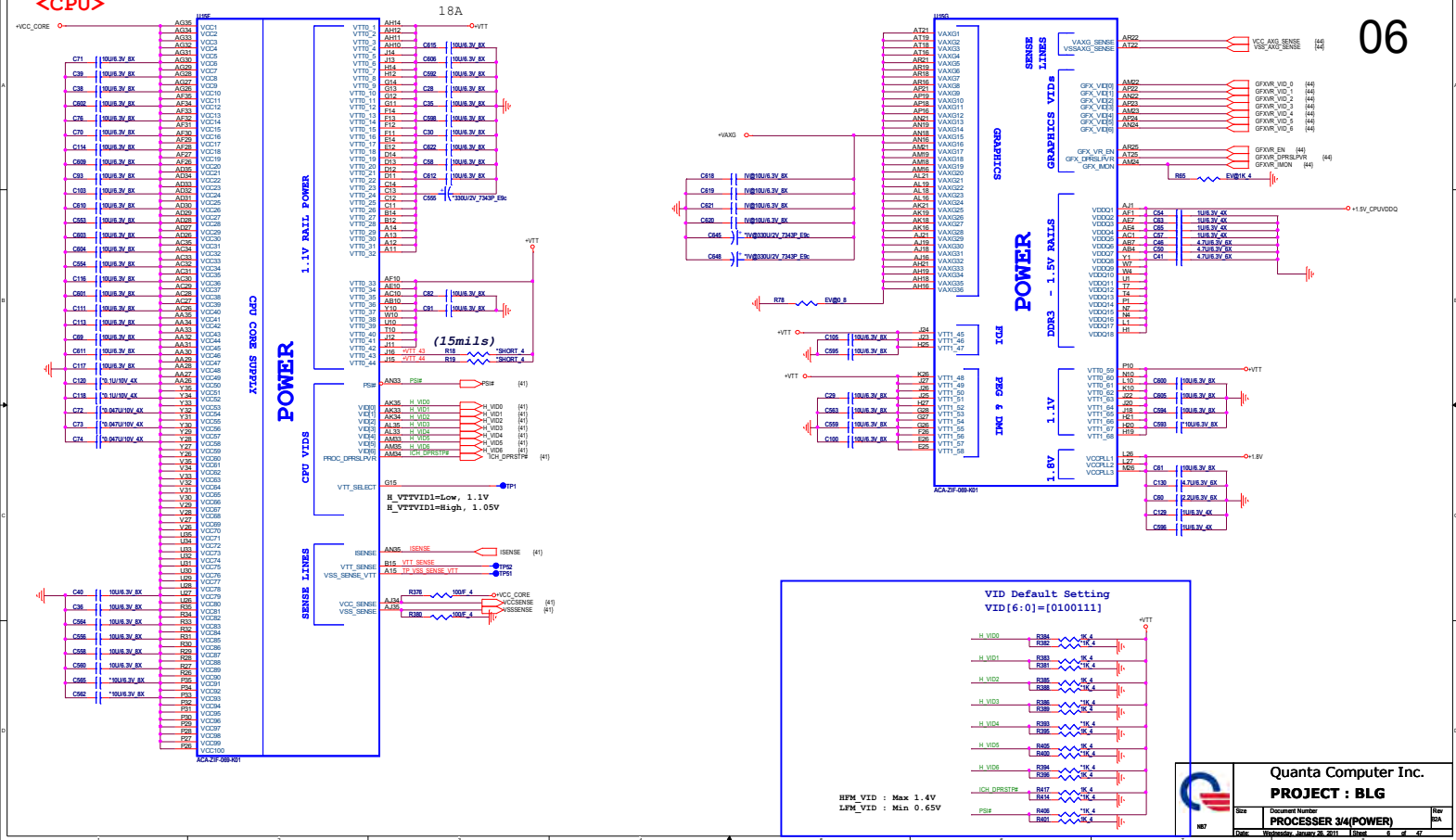
Table of Contents

[illegible]

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

GND PLANE	PAGE
 8769AGND	32
 GND	ALL
 JSL95870A_GPU_AGND	43

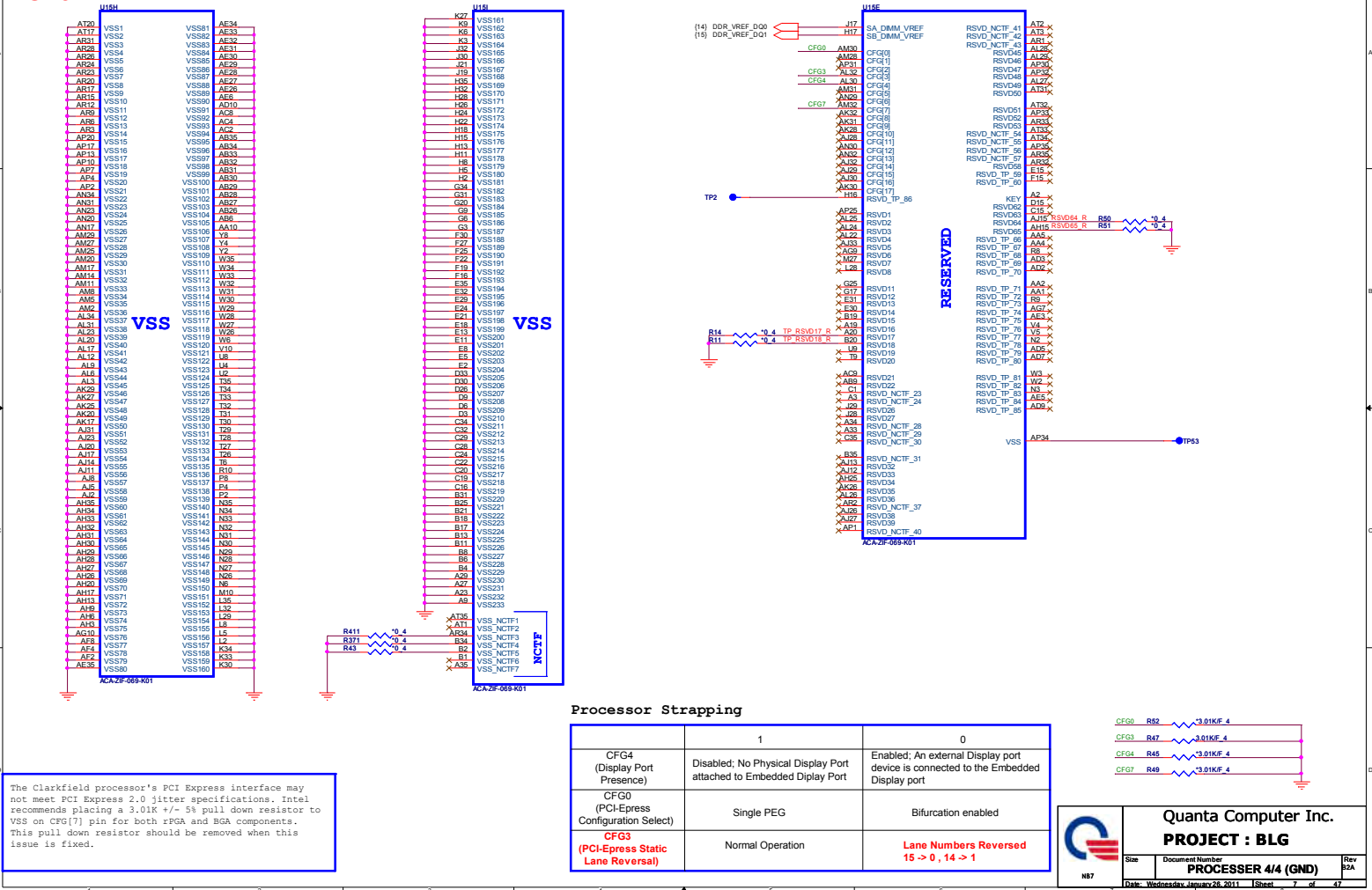




AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

<CPU>



<PWM>



<S3P>



<S3P>



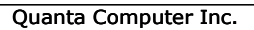
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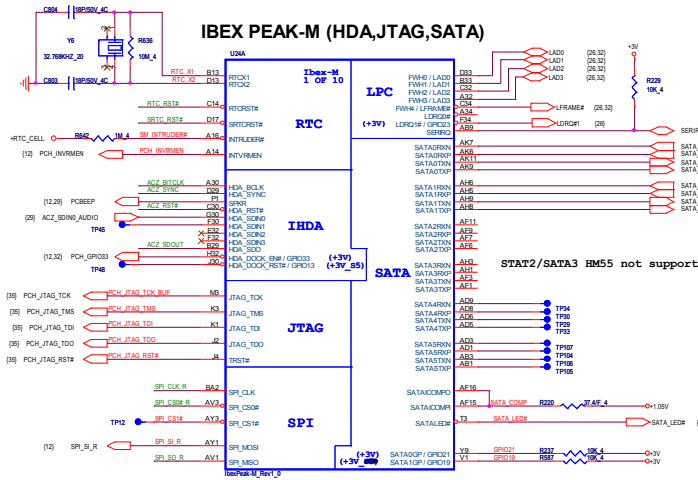


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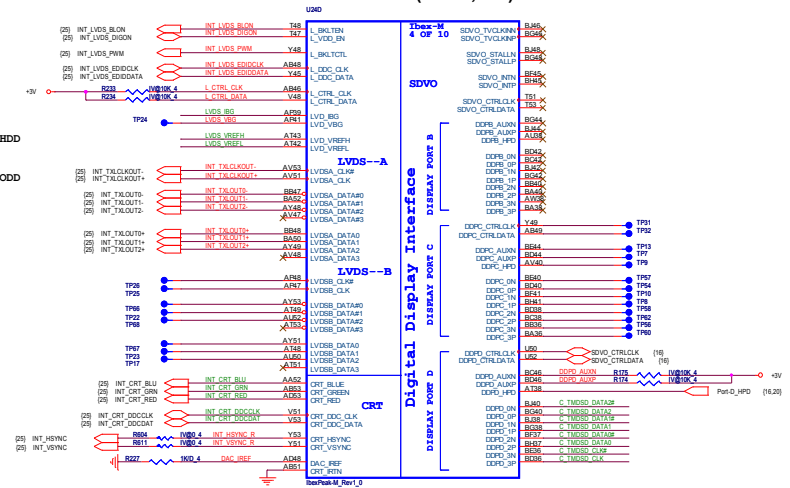


Size	Document Number S3 Power Reduction	Rev B2A
Date: Wednesday, January 26, 2011 Sheet 8 of 47		

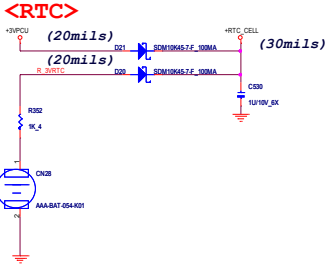
IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M (LVDS,DDI)



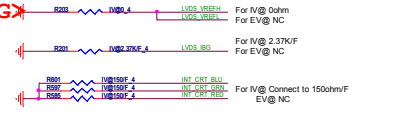
RTC BATTERY



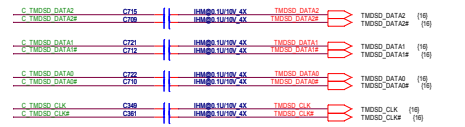
DDP Setting

Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

<CLG>



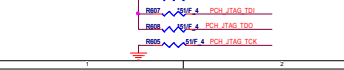
HDMI



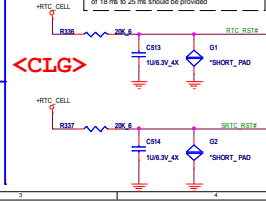
<CLG>



<CLG>

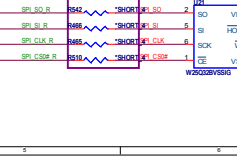


RESET JUMP



4M byte SPI ROM

<CLG> D3B



PCH	2MB	4MB	8MB
PM55			
HM55			
HM57/PM57			
QM57/QS57			

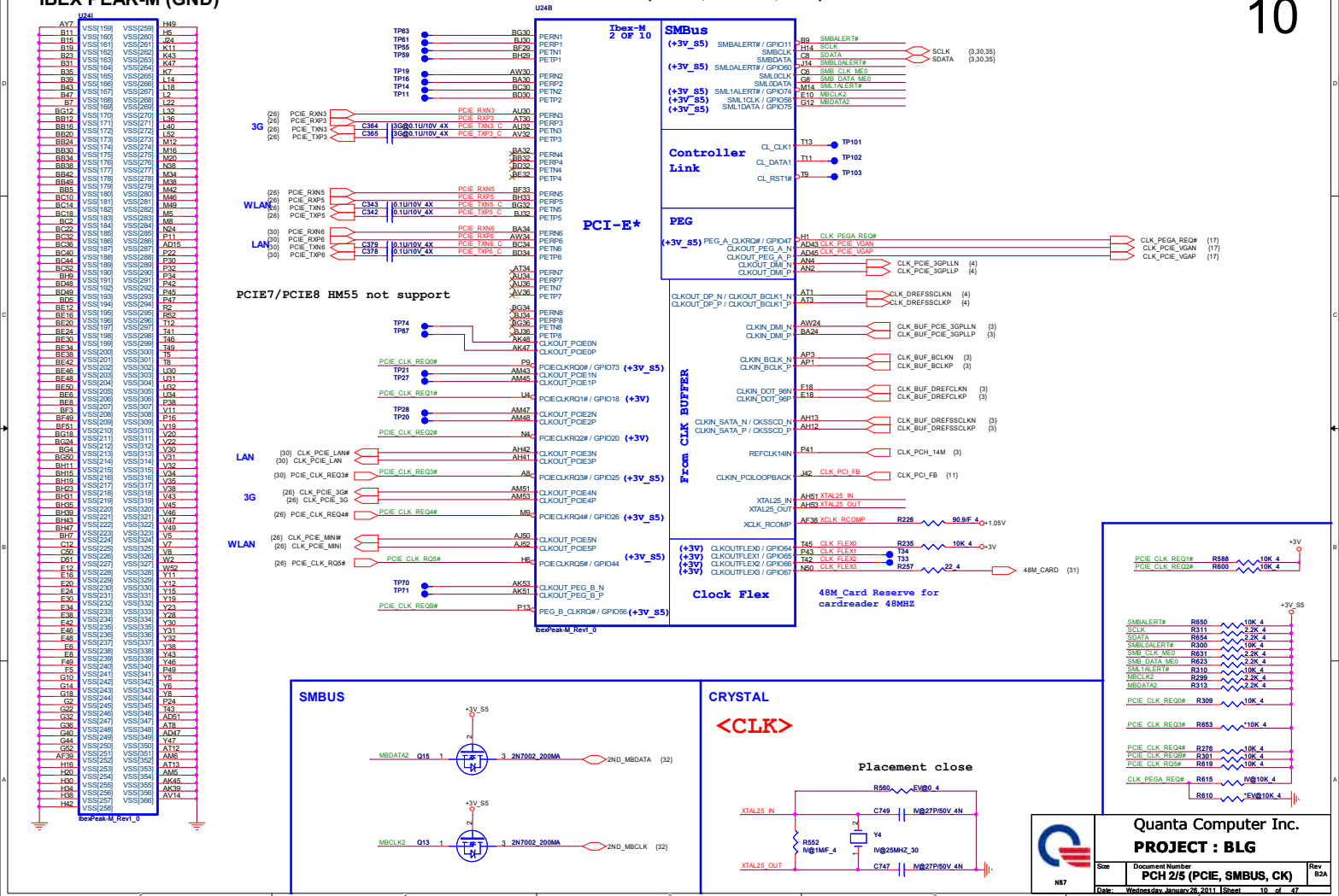
Quanta Computer Inc.

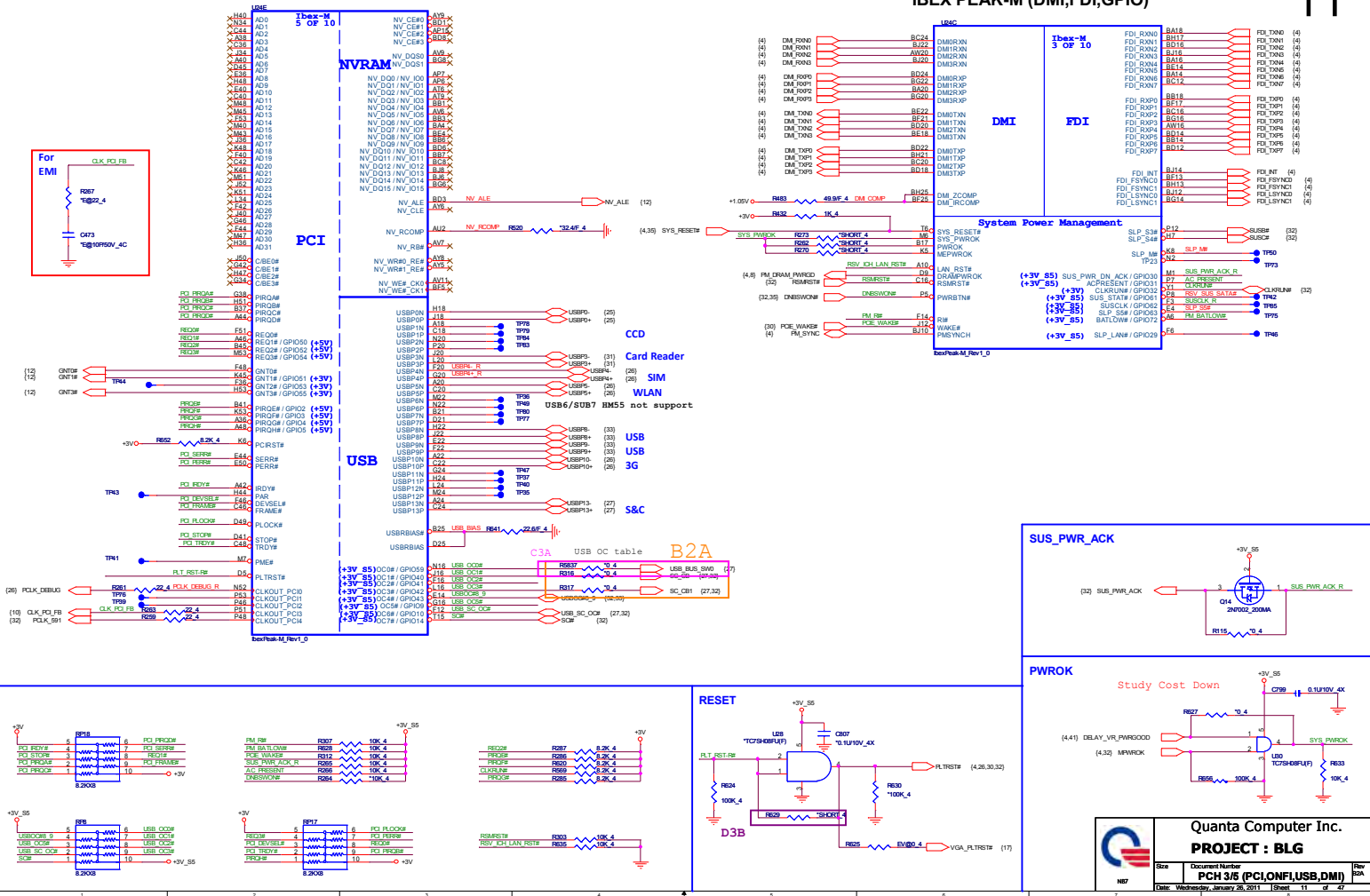
PROJECT : BLG

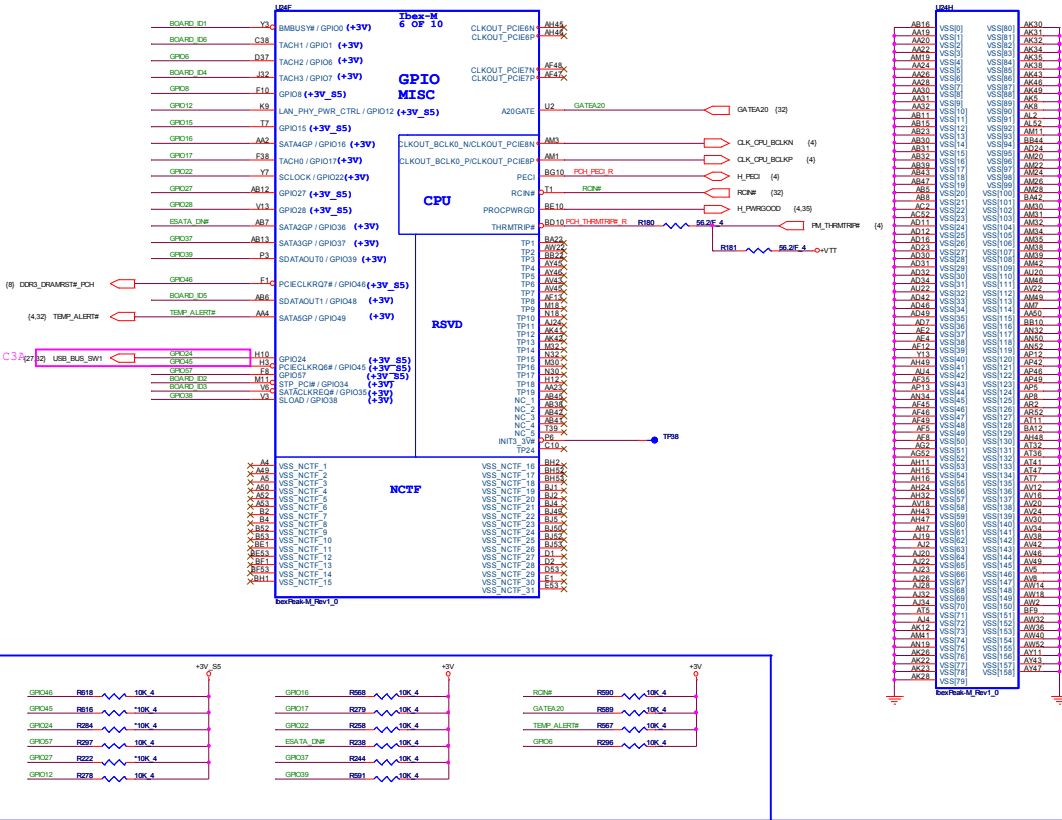
Rev: 1.0

Doc: PCH 1/5 (SATA,HDA,LPC)

Date: Wednesday, January 28, 2010 10:00 AM







BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	GPIO28	GPIO38
UMA SKU	H	L						
VGA SKU			H	L				
W/ MDC								
W/O MDC								
W/ HDMI								
W/O HDMI								
W/ 3G								
W/O 3G								
W/ BT								
W/O BT								
14 or 15								
13								
Q15 SW (2013)								
New SW (2014)								



SPKR

(1,20) PCBEEP R202 10K_4 0-3V

Reboot option at power-up

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/GPIO55

(11) GNT3# R202 10K_4 0-3V

Top-Block Swap Override

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

HDA_DOCK_EN #GPIO33

(9,32) PCH_GPIO33 R202 10K_4 0-3V

Flash Descriptor Security Override

0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

GNT0#/GNT1#

(11) GNT0# R202 10K_4 0-3V

GNT1# R202 10K_4 0-3V

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SP1

SPI_MOSI

(9) SPI_MOSI R204 10K_4 0-3V

TPM Functionality Disable

1 = Enabled
0 = Disable

NV_ALE

(11) NV_ALE R206 10K_4 0-1.8V

Intel Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

1 = Enabled
0 = Disabled (Default)

GPIO8

Reserved

This signal has a weak internal pull-up.
NOTE: This signal should not be pulled low

GPIO15

Reserved

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

R202 10K_4 0-3V

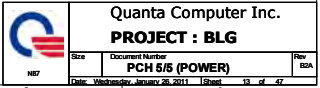
On-Die PLL Voltage Regulator

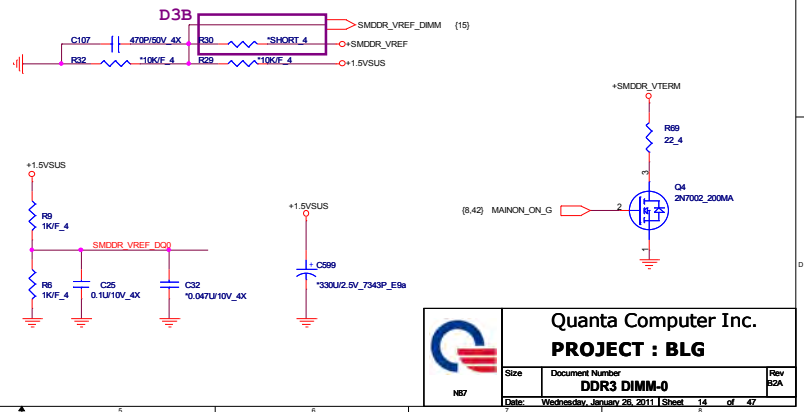
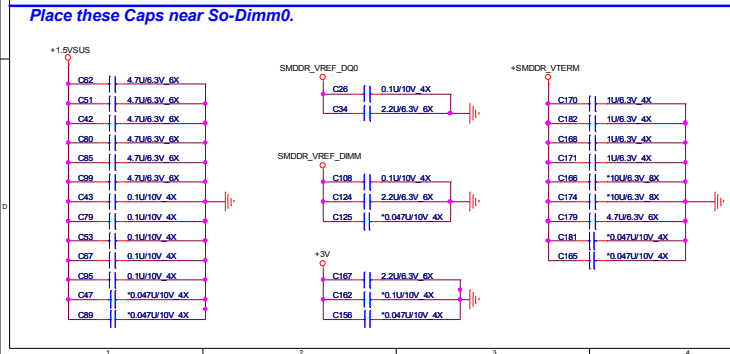
0 = Disables the VccVIRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVIRM to have a clean supply for analog rails.
No need to use on-board filter circuit.
This signal has a weak internal pull-up.

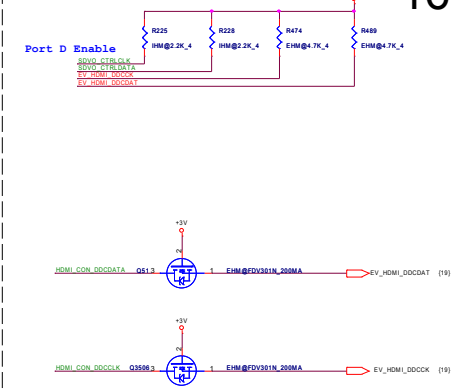
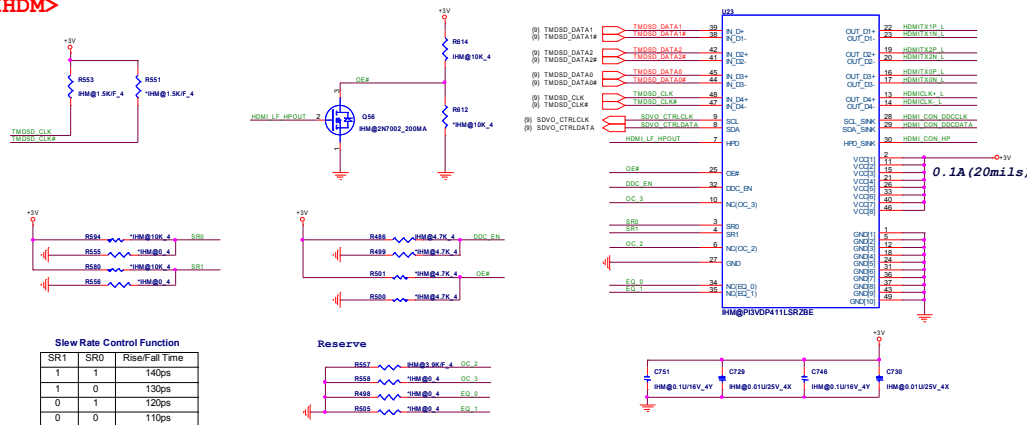
RTC_CELL R244 330K_5 PCH_INVRSEN 0-3V

INTVRSEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRM

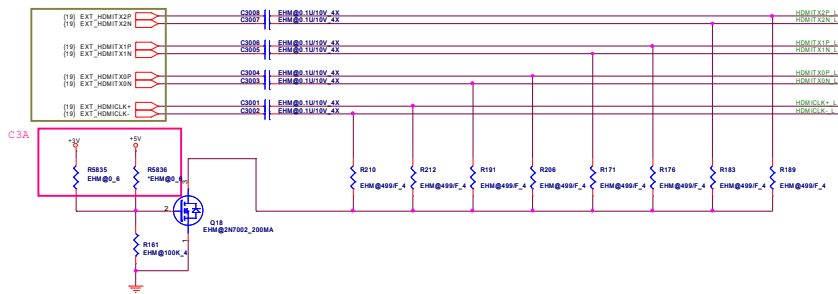
Quanta Computer Inc.
PROJECT : BLG
PCH 4/5 (GPIO & Strap)



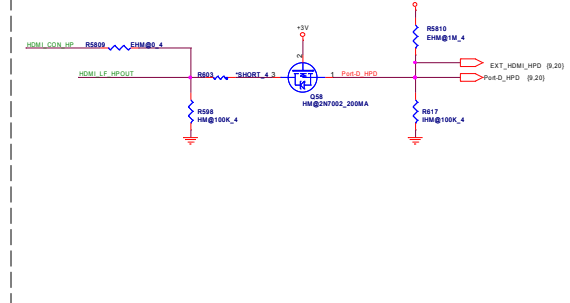




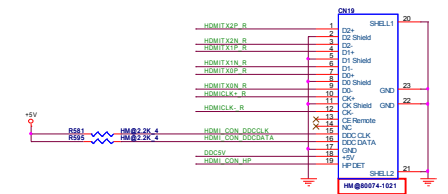
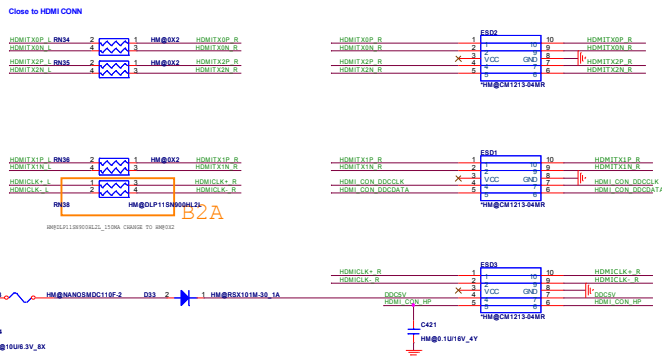
Discrete HDMI

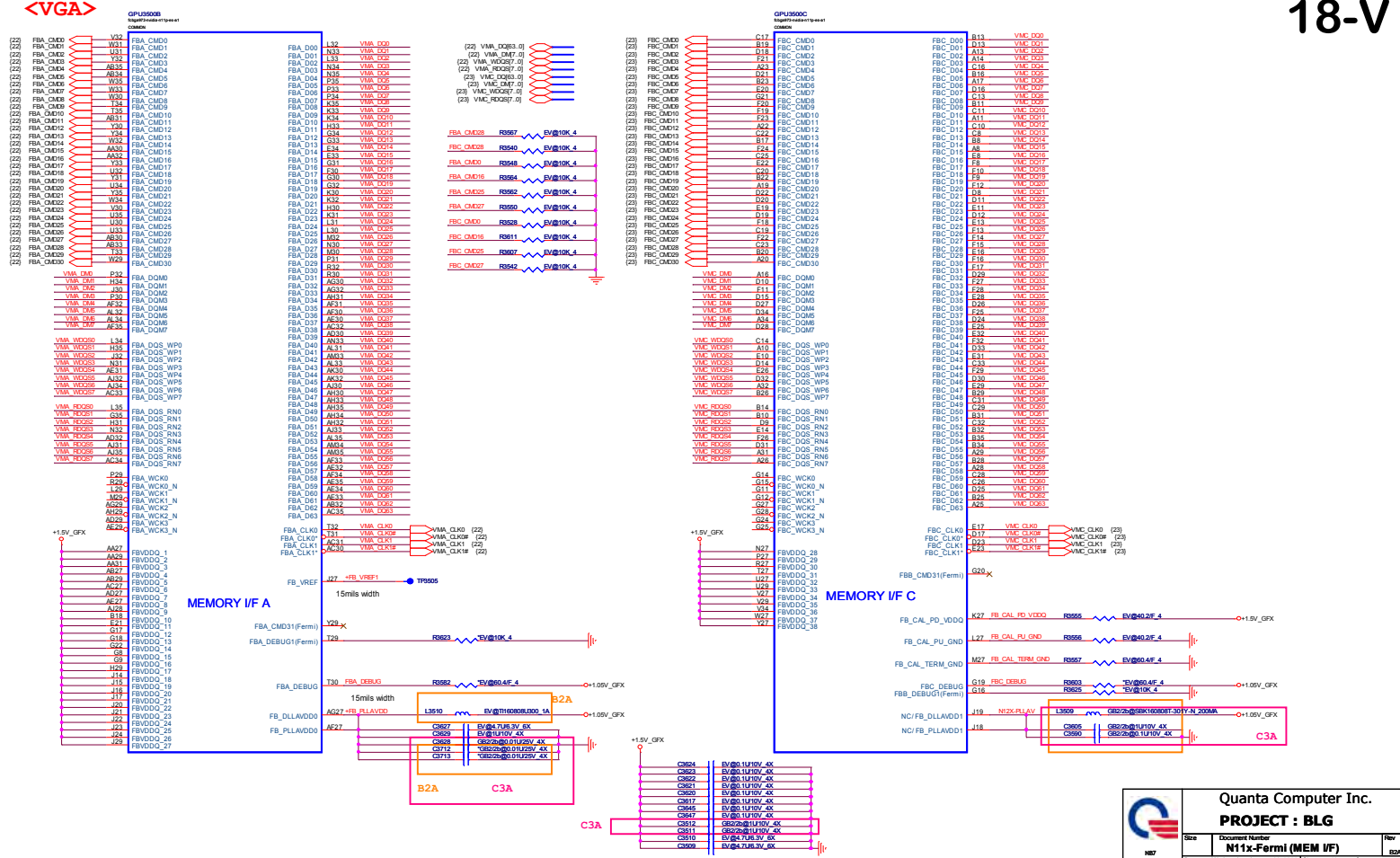



HDMI HPD



FOR EMI



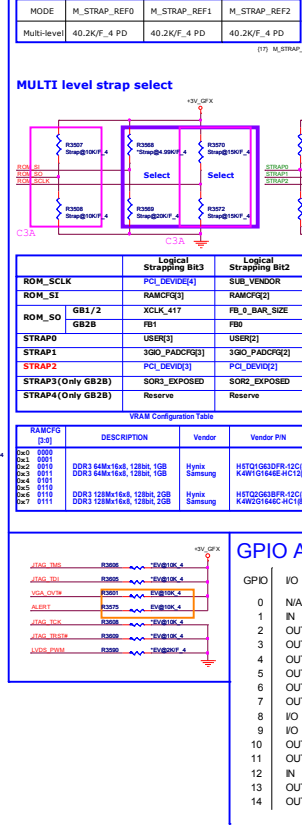
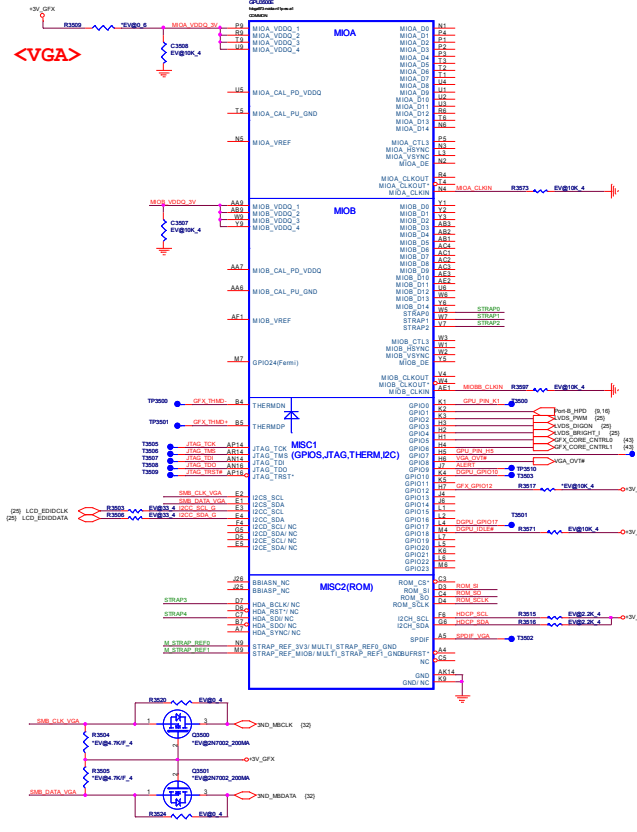




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PROJECT : BLG

Size	Document Number	Rev
	N11x-Fermi (MEM I/F)	
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20-V

Strappin Model select

MODE	M_STRAP_REF0	M_STRAP_REF1	M_STRAP_REF2
Multi-level	40.2K/F_4 PD	40.2K/F_4 PD	40.2K/F_4 PD

(17) M_STRAP_REF2

MULTI level strap select

GPIO ASSIGNMENTS

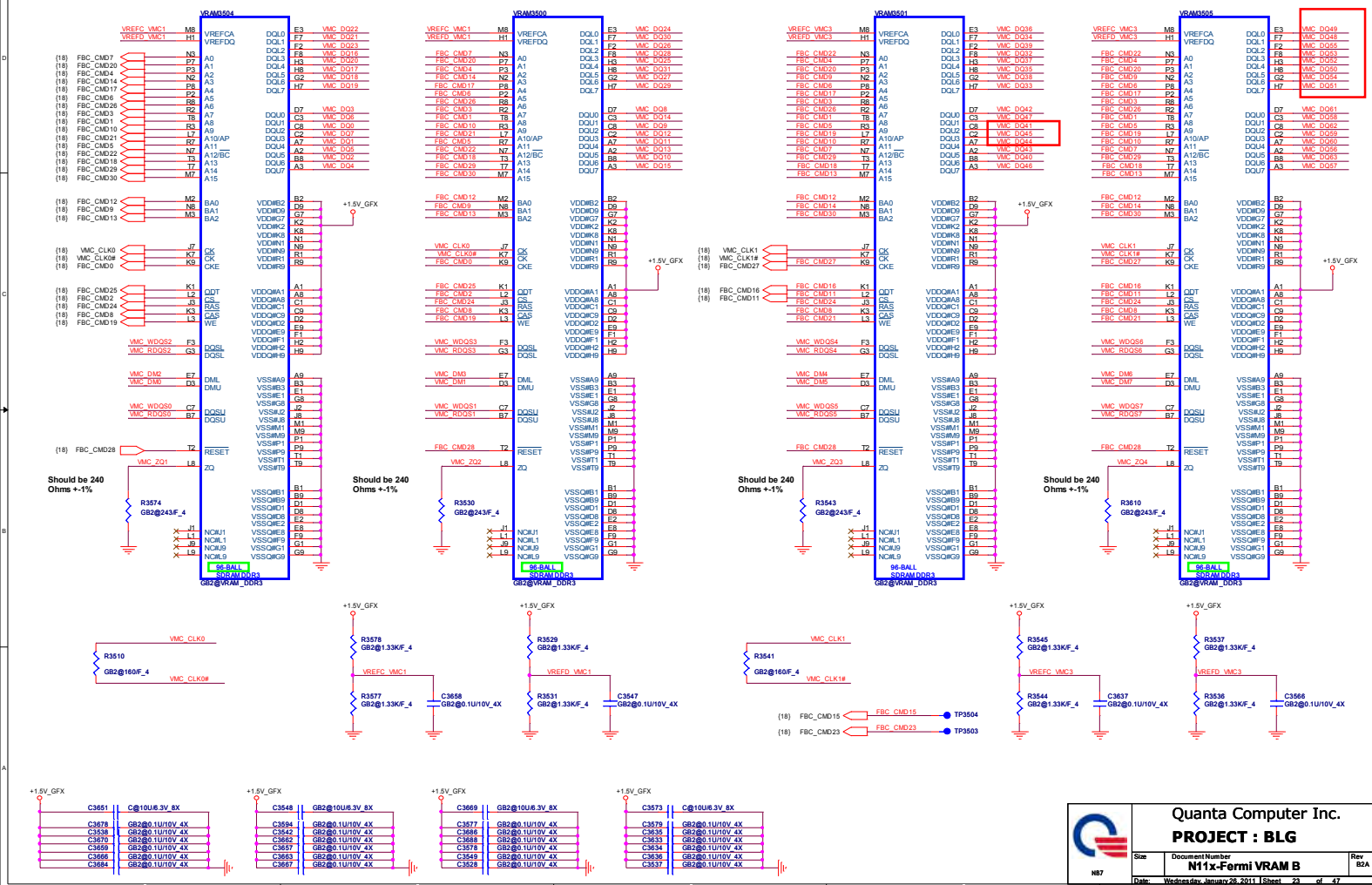
GPIO	IO	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for I/F link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	IO	LOW	OVERT
9	IO	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLISYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

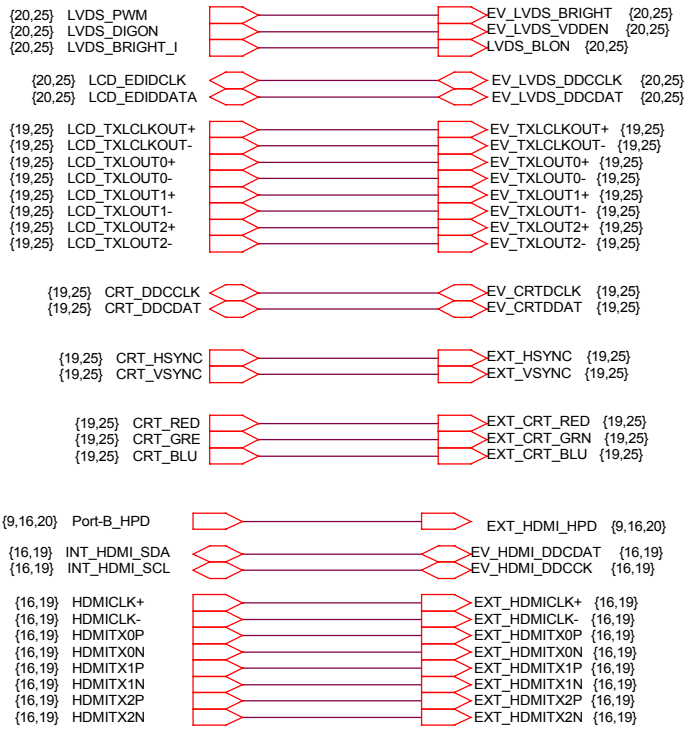
VRAM Configuration Table


RAMCFG	DESCRIPTION	Vendor	Vendor PIN	ICM_B1
0x0 0000				
0x2 0001				
0x2 0010	DDR3 64Mx16x8, 128Mx10B	Hynix	H1ST015603F9-DC(800MHz) / H1ST015603F9-1C(800MHz)	PD 15K
0x3 0011	DDR3 64Mx16x8, 128Mx10B	Samsung	K4W015646E-NC(1200MHz) / K4W015646E-NC(1000MHz)	PD 50K
0x4 0101				
0x4 0110	DDR3 128Mx16x8, 128Mx20B	Hynix	H1ST020403F9-DC(800MHz) / H1ST020403F9-1C(800MHz)	PD 35K
0x7 0111	DDR3 128Mx16x8, 128Mx20B	Samsung	K4W021546C-NC(1200MHz) / K4W021546C-NC(1000MHz)	PD 45K

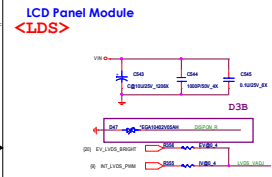
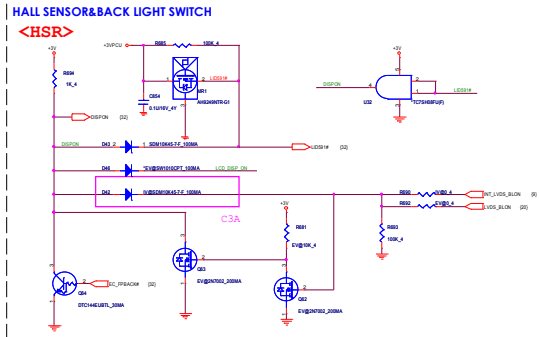
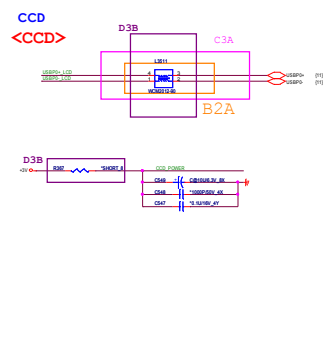
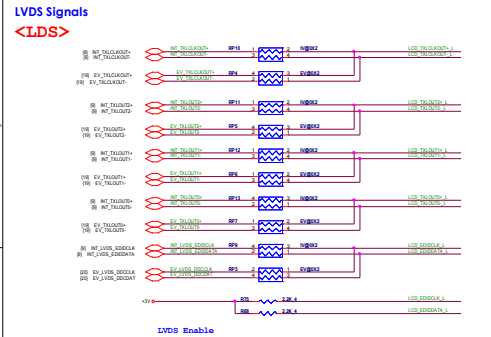
Logical Strap Bit Mapping

PU-VDD	PD
5K	1000
10K	1001
15K	1010
20K	1011
25K	1100
30K	1101
35K	1110
40K	1111

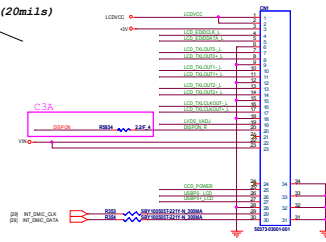




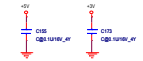
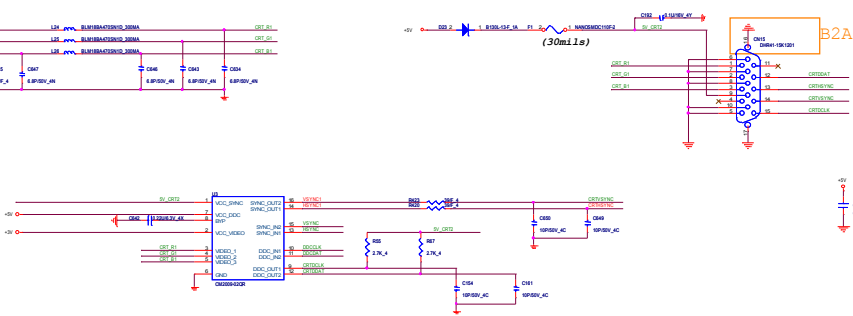
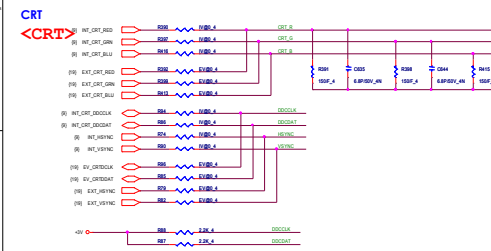
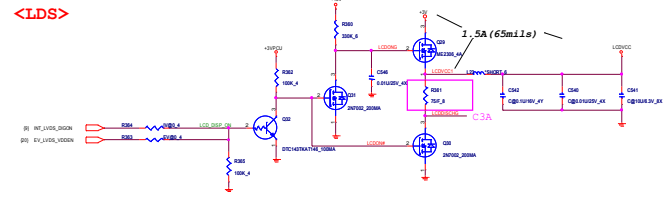
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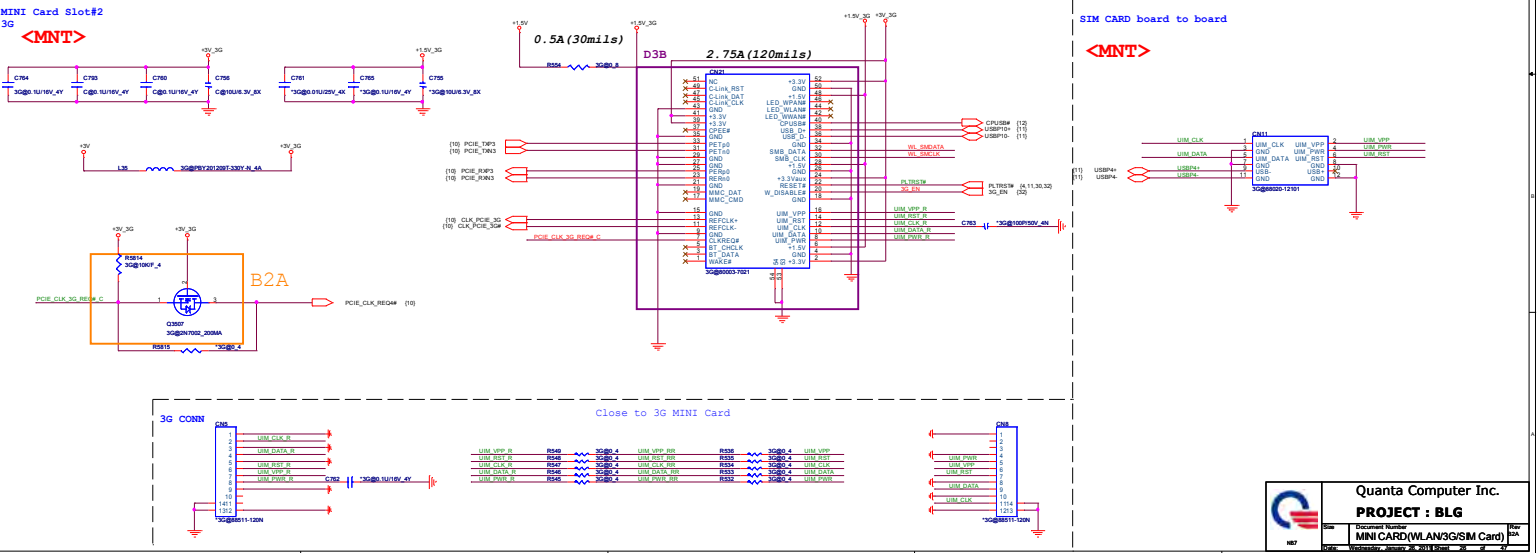


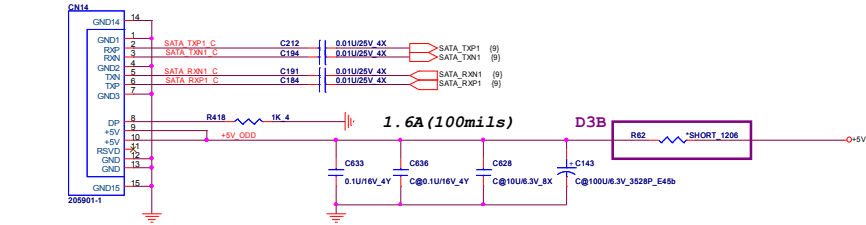
0.3A (20mils)



LCD POWER SWITCH



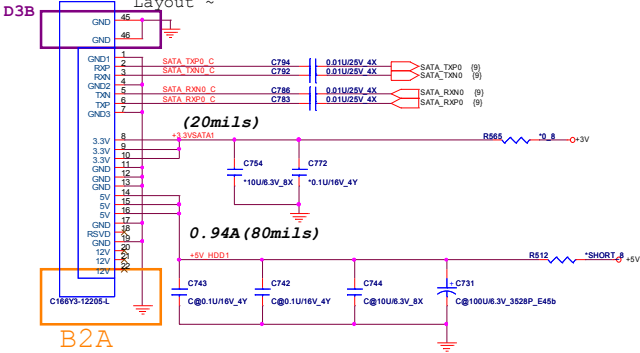




SATA HDD

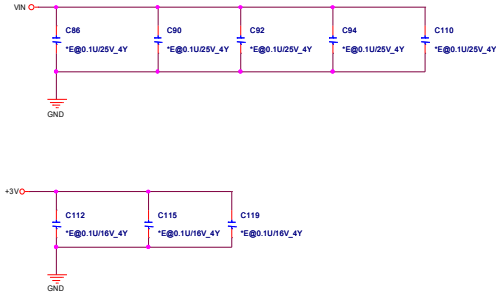
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Take care SATA trace Length

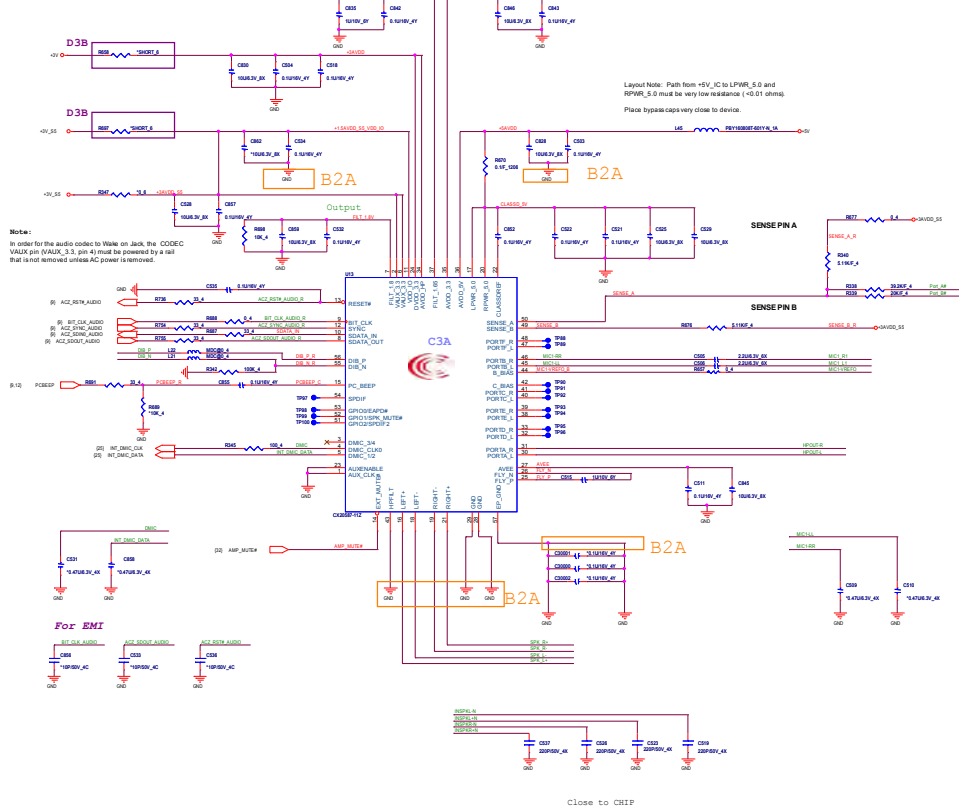


EMI

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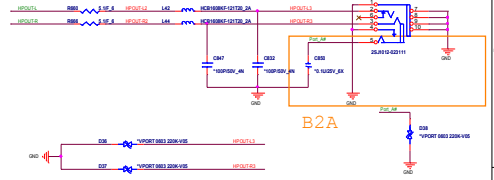


	Quanta Computer Inc.	
	PROJECT : BLG	
NB7	Size	Document Number
		HDD/ODD/EMI
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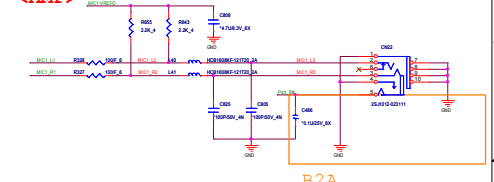
Earphone

<AMP>



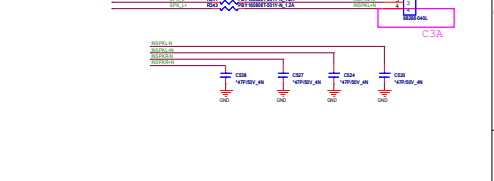
External MIC

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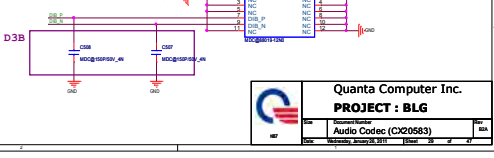


Internal Speaker

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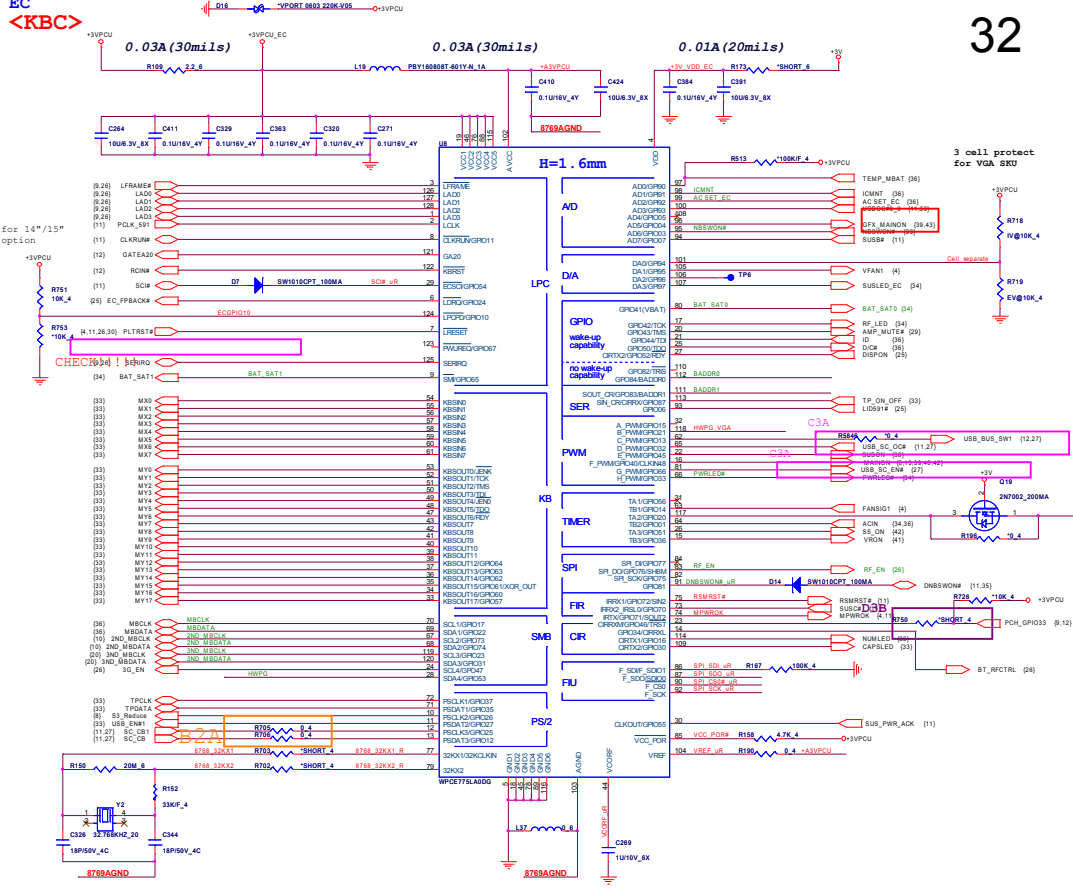


MDC <MDC>



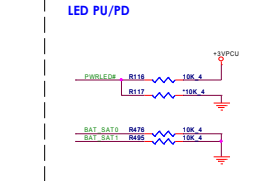
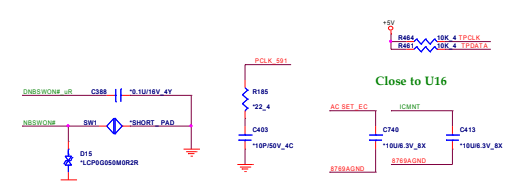
Quanta Computer Inc.
PROJECT : BLG
Audio Codec (CX20587)





SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	POH SML1	
2	AMD SMBus	SB1
2	EC EEPROM	AG1
3	VGA Board Thermal Sensor	SB1



SM BUS PU

0.03A (30mils)

0.01A (20mils)

I/O Base Address

I/O Address	
Index	Data
BADDR10	0 0
BADDR11	0 1
BADDR12	1 0
BADDR13	1 1

ID

0.003A (20mils)

SPI FLASH

0.025A (20mils)

INTERNAL KEYBOARD STRIP SET

HWPG

Quanta Computer Inc.

PROJECT : BLG

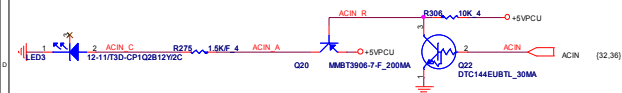
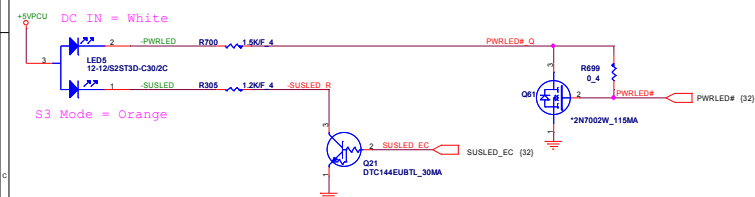
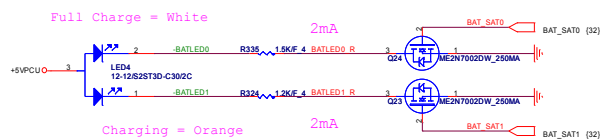
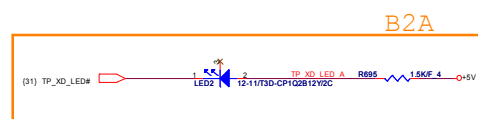
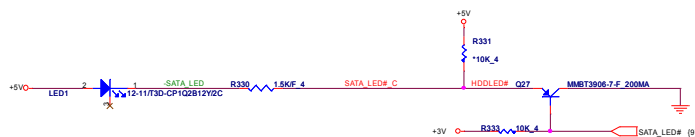
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Document Number: EC-WPC8763LDG/WPC8769L(O)

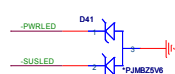
Rev: 55A

Date: Wednesday, August 28, 2013 11:00am

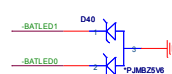
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LED <LED>**AC-IN****POWER****BATTERY****CARDREADER****HDD/ODD****ESD Protect**

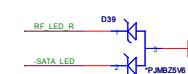
FOR POWER LED



FOR BATTERY LED



FOR HDD/RF LED



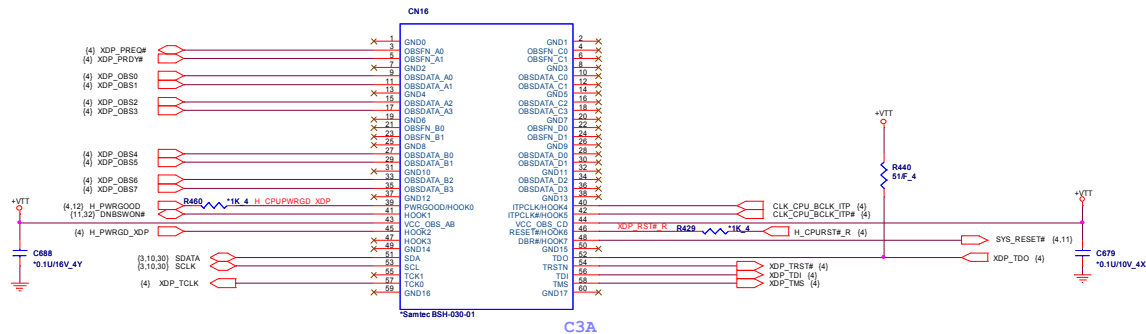
FOR CARDREADER LED



C3A

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	PROJECT : BLG		
	Size	Document Number	Rev
	NB7	LED	B2A

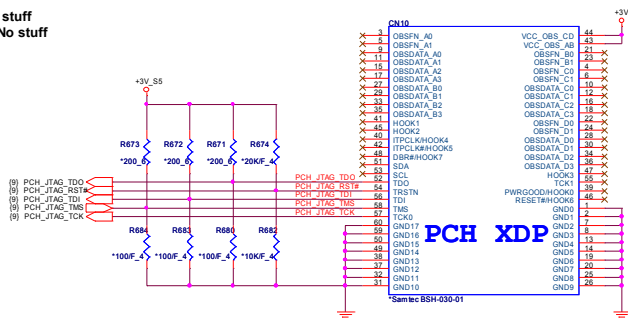
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Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

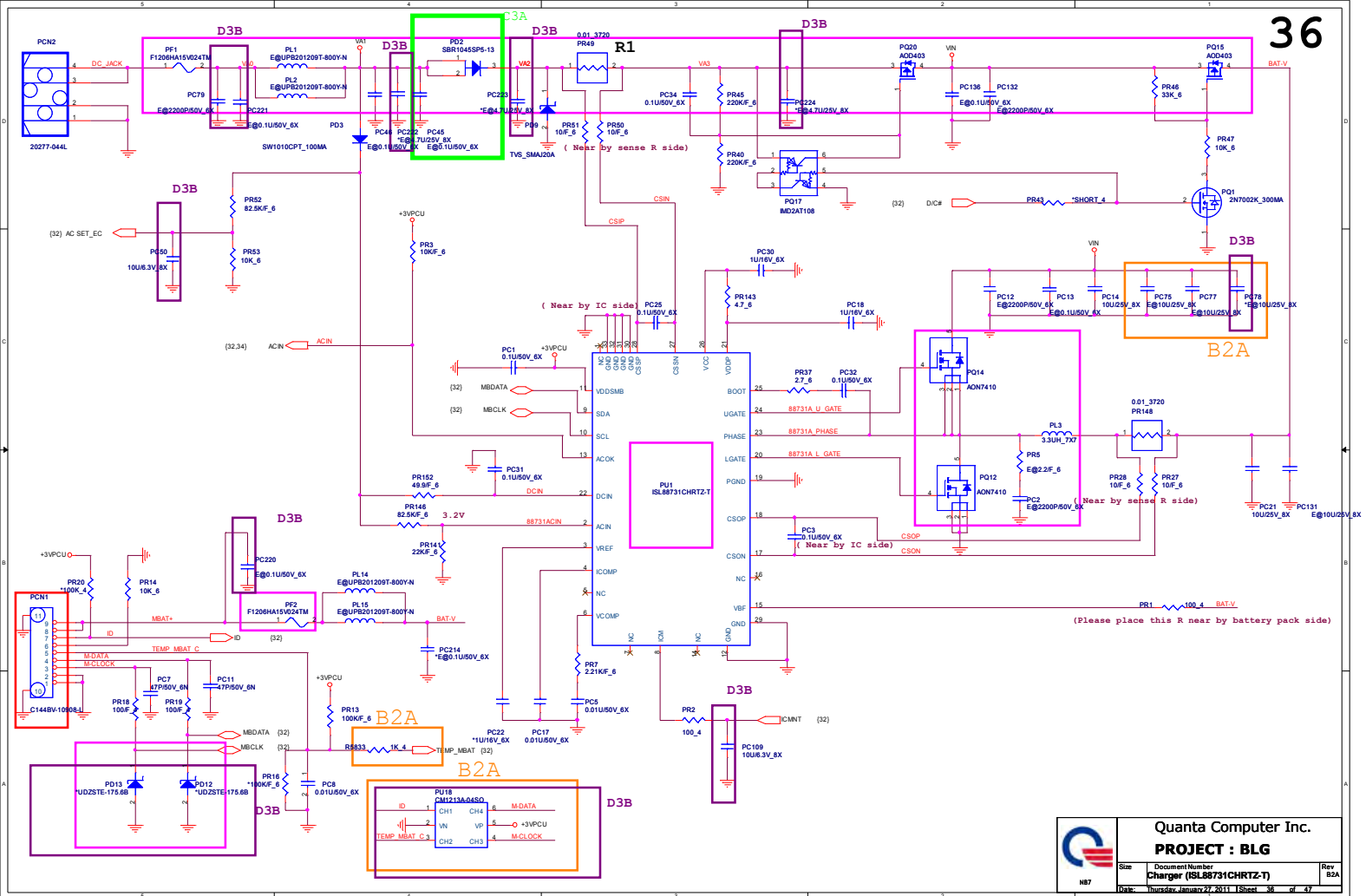
PCH XDP
<SLG>

Note: For ES1/ES2 version all stuff
Production version all No stuff



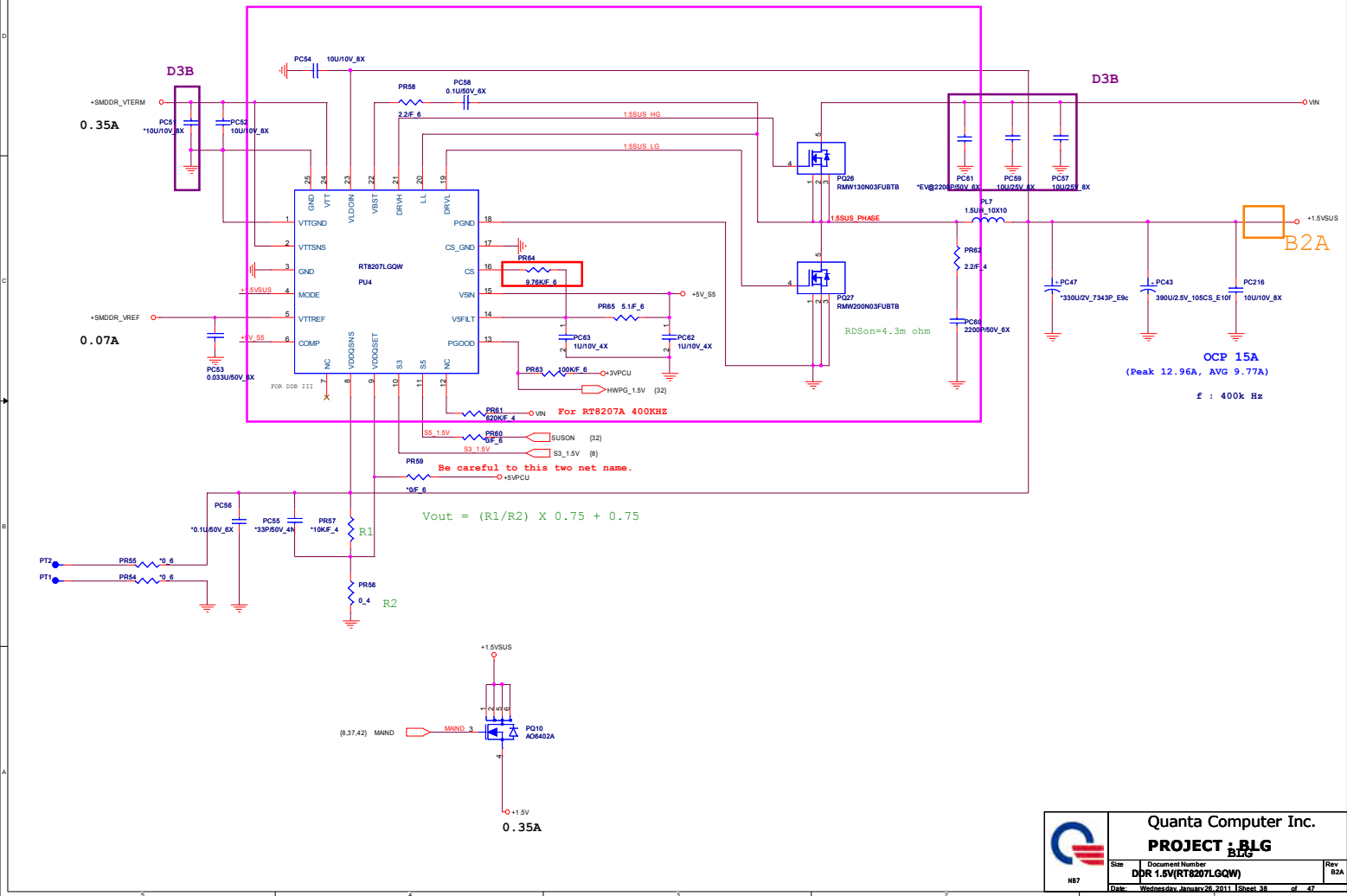
Quanta Computer Inc.
PROJECT : BLG

Size	Document Number	Rev
N87	NVRAM Connector	B0A
Date: Wednesday, January 26, 2018	Sheet: 35	of 47

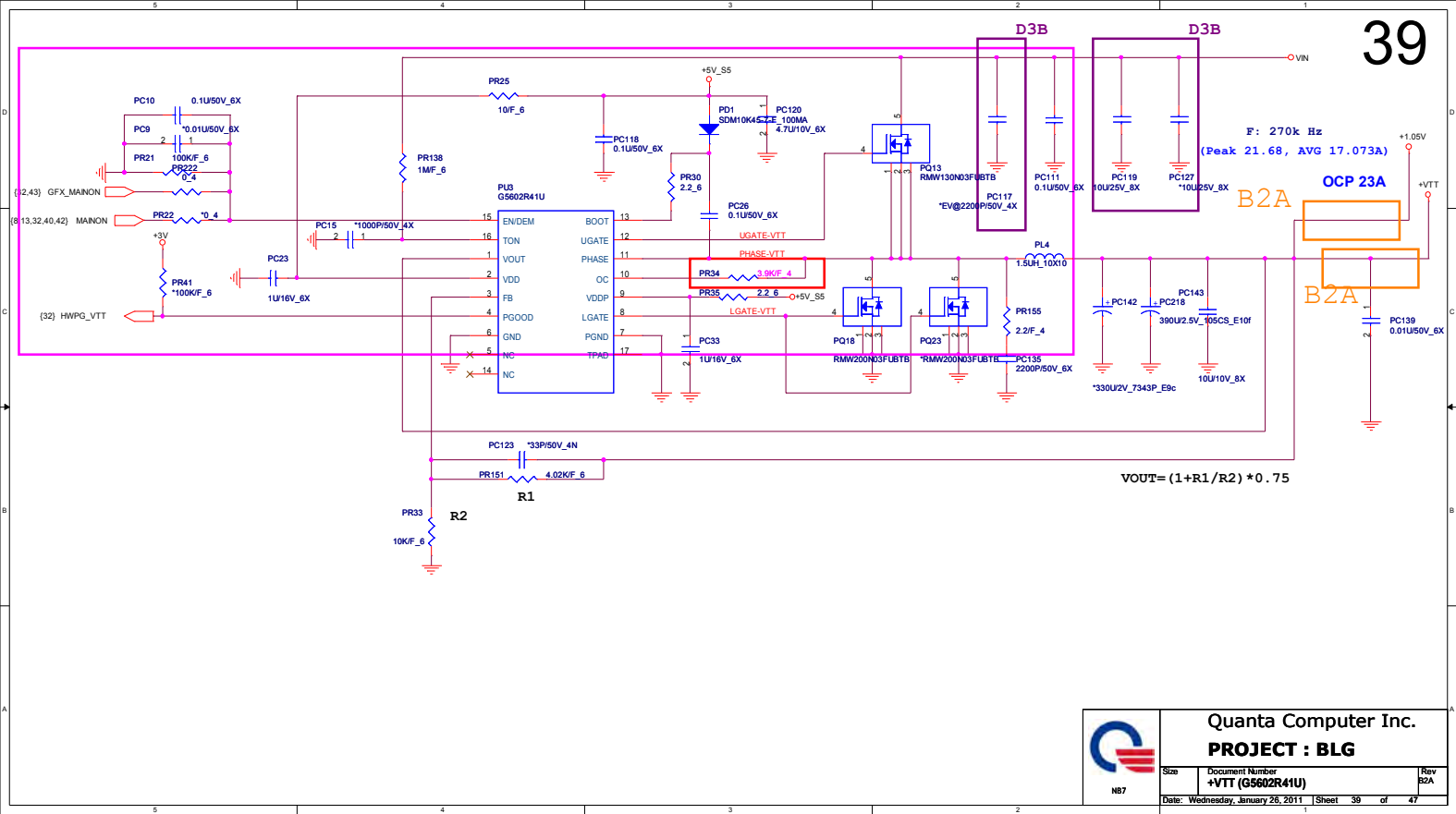



NB7	Quanta Computer Inc.		
	PROJECT : BLG		
	Size	Document Number	Rev
		Charger (ISL88731CHRTZ-T)	B2A

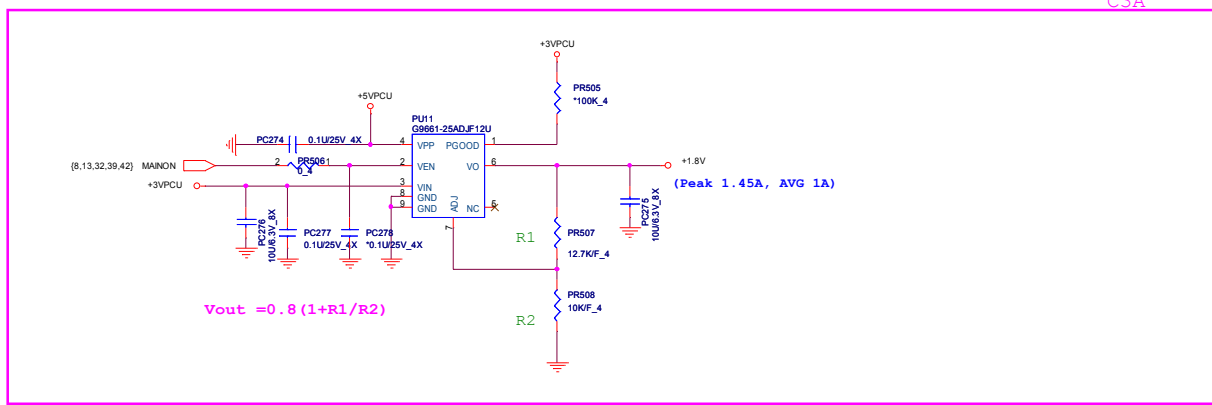
Date: Thursday, January 27, 2011 | Sheet 36 of 47



Quanta Computer Inc.	
PROJECT : RLG	
BLC	
Size	Document Number
Size	DPR 1.5V(RT8207LQGW)
Date	Released: January 26, 2011 (Sheet 38 of 47)
Rev	B2A



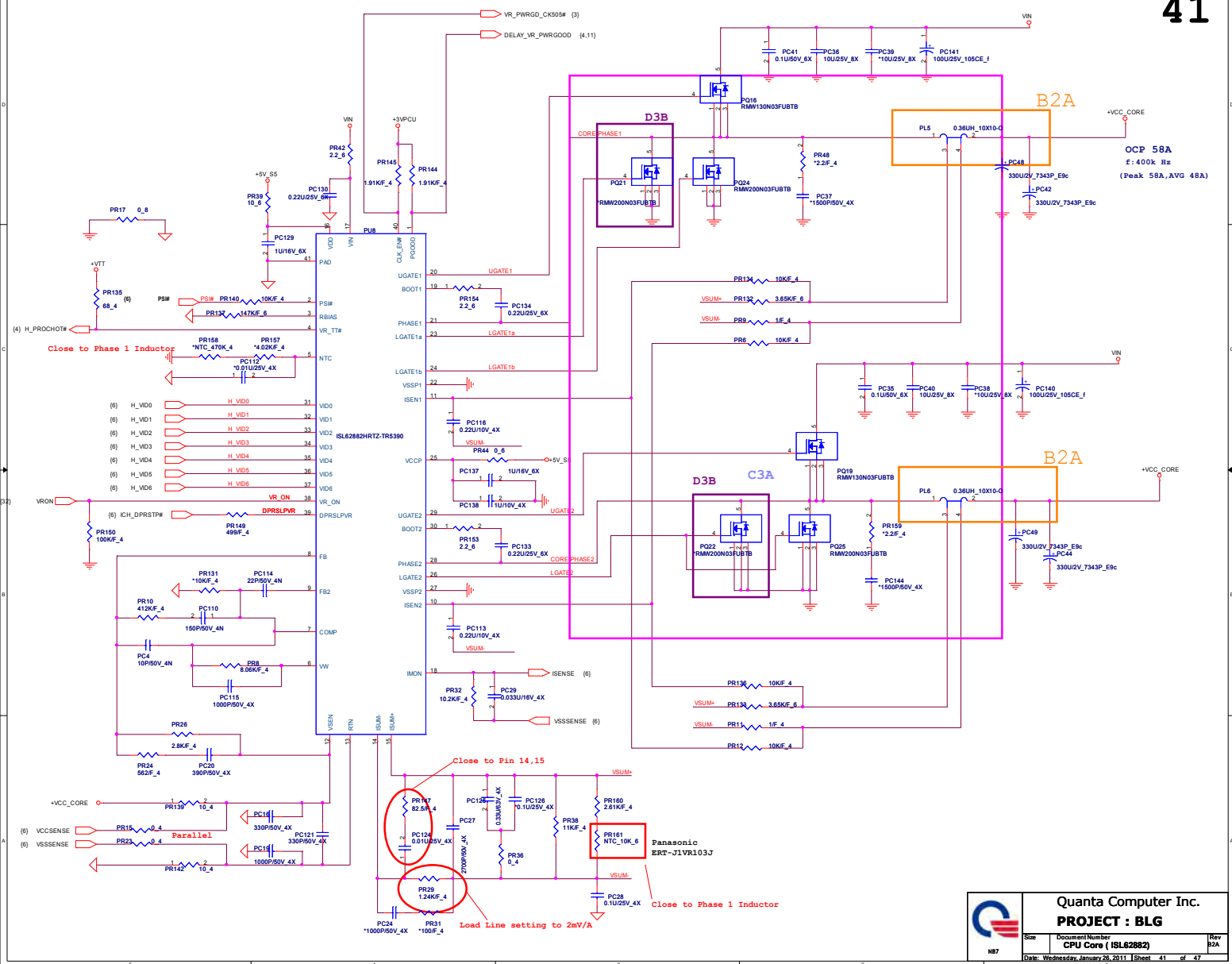
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Size	Document Number	Rev	
NB7	+VTT (G5602R41U)	B2A	
Date: Wednesday, January 26, 2011	Sheet 39 of 47		

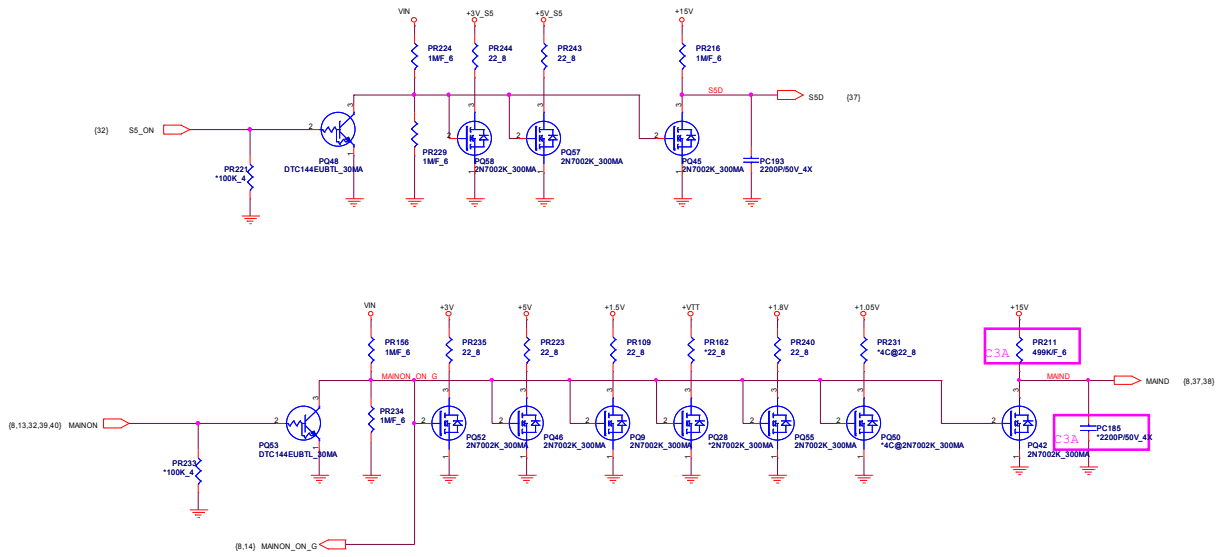


Quanta Computer Inc.

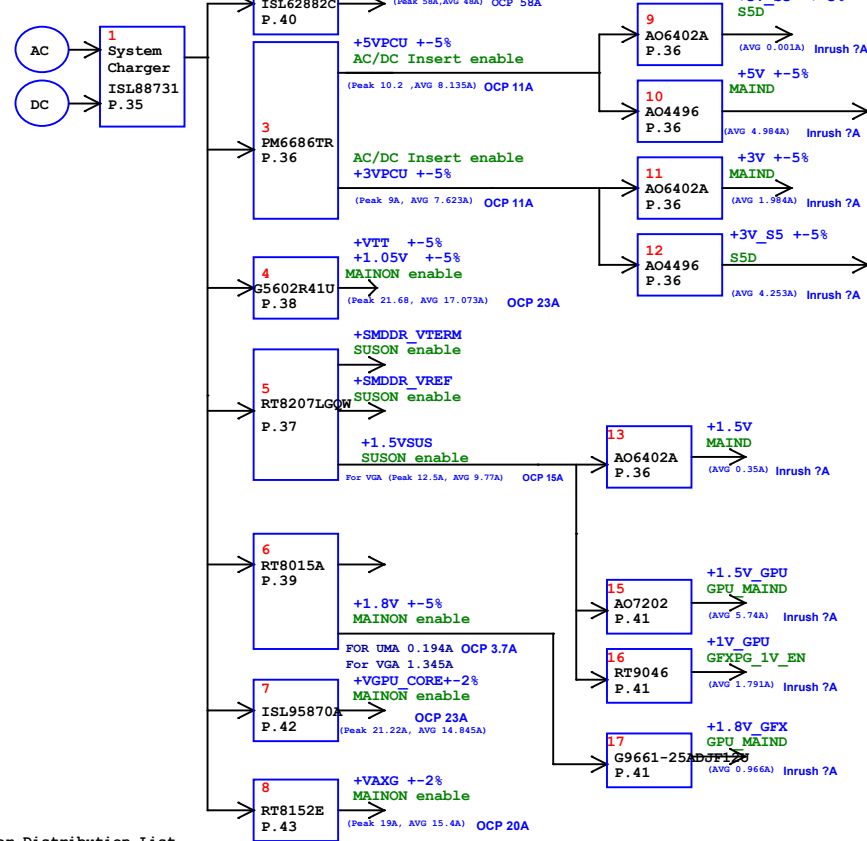
PROJECT : BLG

Size	Document Number	Rev
	+1.8V (G9661-25ADJF12U)	B2A
Date: Wednesday, January 26, 2011 Sheet 40 of 47		





Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : BLG

Size	Document Number	Rev
107	Power Tree Table	EDA
Date: Wednesday, August 28, 2019 Sheet 45 of 47		

